FOSS TCAD/EDA Platform for Compact Modeling

Date: Mon. 26th Nov.
Time: 1:30 pm
Location: Building 59, Room 2003

Speaker:

Dr. Wladek Grabinski
Consultant SPICE.
Grabinski Modeling Consulting

Abstract:

Compact/SPICE models of circuit elements (passive, active, MEMS, RF) are essential to enable advanced IC design using nanoscaled semiconductor technologies. Compact/SPICE models are also a communication means between the semiconductor foundries and the IC design teams to share and exchange all engineering and design information. To explore all related interactions, we are discussing selected FOSS CAD tools along complete technology/design tool chain from nanascaled technology processes; thru the MOSFET, FDSOI, FinFET and TFET compact modeling; to advanced IC transistor level design support. New technology and device development will be illustrated by application examples of the FOSS TCAD tools: Cogenda TCAD and DEVSIM. Compact modeling will be highlighted by review topics related to its parameter extraction and standardization of the experimental and measurement data exchange formats. Finally, we will present two FOSS CAD simulation and design tools: ngspice and Qucs. Application and use of these tools for advanced IC design (e.g. analog/RF IC applications) directly depends the quality of the compact models implementations in these tools as well as reliability of extracted models and generated libraries/PDKs. Discussing new model implementation into the FOSS CAD tools (Gnucap, Xyce, ngspice and Qucs as well as others) we will also address an open question of the compact/SPICE model Verilog-A standardization. We hope that this presentation will be useful to all the researchers and engineers actively involved in the developing compact/SPICE models as well as designing the integrated circuits in particular at the transistor level and then trigger further discussion on the compact/SPICE model Verilog-A standardization and development supporting FOSS CAD tools.

Bio:

Wladek Grabinski received the Ph.D. degree from the Institute of Electron Technology, Warsaw, Poland, in 1991. From 1991 to 1998 he was a Research Assistant at the Integrated Systems Lab, ETHZ, Switzerland, supporting the CMOS and BiCMOS technology developments by electrical characterization of the processes and devices. From 1999 to 2000, he was with LEG, EPFL, and was engaged in the compact MOSFET model developments supporting numerical device simulation and parameter extraction. Later, he was a technical staff engineer at Motorola, and subsequently at Freescale Semiconductor, Geneva Modeling Center, Switzerland. He is now a consultant responsible for SPICE modeling, characterization and parameter extraction of MOST devices for the analog/RF IC applications. He is currently consulting on the development of next generation compact models for the nanoscaled technology very large scale integration (VLSI) circuit simulation. His current research interests are in high-frequency characterization, compact modeling and its Verilog-A standardization as well as device numerical simulations of MOSFETs for analog/RF low power IC applications. He is an editor of the reference modeling book Transistor Level Modeling for Analog/RF IC Design and also authored or coauthored more than 50 papers. Wladek is the chair of the ESSDERC Track4: "Device and Circuit Compact Modeling" as well as has served as a member of organization committee of ESSDERC/ESSDERC, TPC of SBMicro, SISPAD, MIXDES Conferences; reviewer of the IEEE TED, IEEE MWCL, IJNM, MEE, MEJ. He is a Member At Large of Swiss IEEE ExCom and also supports the EPFL IEEE Student Branch acting as its Interim Branch Mentor. Wladek is involved in activities of the MOS-AK Association and serves as a coordinating manager since 1999.