Hardware Implementation of Digital Communication Systems on FPGA Board

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Objective

a digital communication system will be simulated on a software (MATLAB) and also emulated on a Field Programmable Gate Array (FPGA) board, to justify that the use of hardware-based technology can greatly enhance the execution time as well as reduce the complexity of the system. Therefore, the performance of the system will be evaluated through the Bit Error Rate and the execution time.

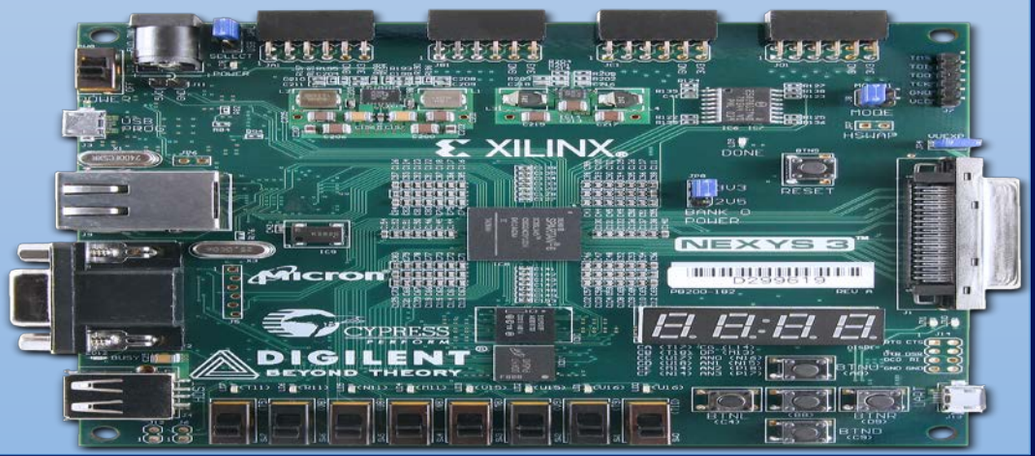
Motivation

Many modern techniques, such as Multiple-Input Multiple-Output (MIMO) and Orthogonal Frequency Division Multiplexing (OFDM) rely on heavy and complex processing both at the transmitter and receiver side. Giving rise to higher demands on fast and efficient computational tools, since the use of conventional software simulations can take significant amounts of time. Therefore, the exploitation of FPGA boards has proven to be an attractive solution for the implementation and emulation of new evolving technologies.

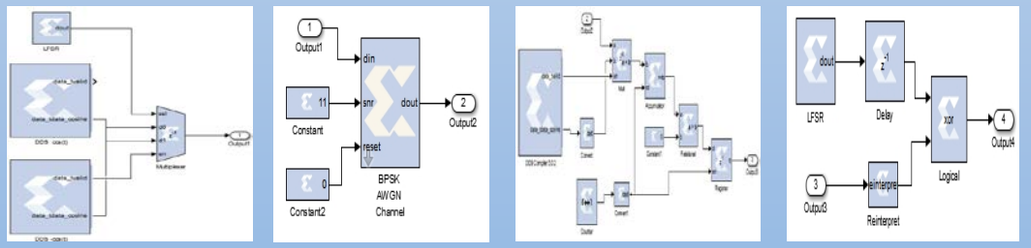
Background

A Binary Phase Shift Keying (BPSK) digital communication system embeds the information in the phase of two carriers that are shifted by180^0. The transmitted signal will be corrupted by an Additive White Gaussian Noise (AWGN). At the receiver side, an optimum receiver that employs Maximum Likelihood detection using a correlator to detect the transmitted signal. The Bit Error Rate is defined as the total number of errors divided by the total number of transmitted bits.

FPGA Board

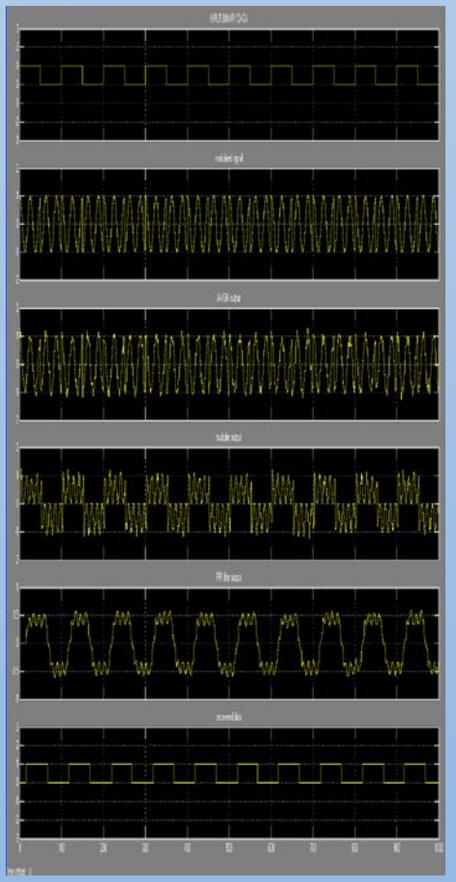


System Generator Model:

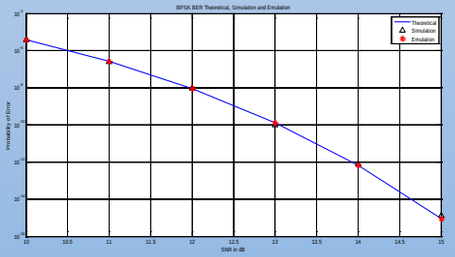


Modulator Channel Demodulator Detection

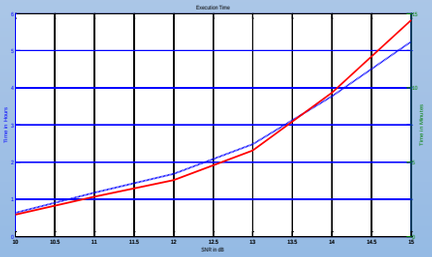
Output Waveforms



Bit Error Rate



Execution Time



Results

The use of hardware-based emulation (FPGA) has improved the execution time required for the Bit Error Rate simulation for higher Signal-to-Noise Ratios. The precision of the BER can be increased further with an increase in execution time that is considered to be less than the software simulation's time by several orders of magnitude.