King Fahd University of Petroleum and Minerals

Electrical Engineering Department

EE200: Digital Logic Circuit Design
*Course Coordinator: Dr. **Mahmoud M. Dawoud***
First Semester 2009-2010 (091)

A. Course Information

Text Book:	**Digital Design (3rd Edition) by M. M. Mano**				
Course	Name		Office	Phone	Sections
Coordinator:	Dr. Mahmoud M. Dawoud **,** ***mmdawoud@kfupm.edu.sa***		59/2070	2299	
Instructors:	Your Section Instructor is: Dr. Mahmoud M. Dawoud **,** ***mmdawoud@kfupm.edu.sa***		59/2070	2299	01
Lab	Name		Office	Phone	Sections
Coordinator:	Dr. Muhammad Al-Sunaidi, ***msunaidi@kfupm.edu.sa***		59-2087	2776	
Instructor:	Your lab. Instructor is: ***_____ @kfupm.edu.sa***				
Grading:	Assignments and Quizzes	Laboratory	Design Project	Two Majors	Final
	15%	20%	5%	30%	30%
	First Major	Second Major	Lab Final		Final
Exams Dates:	**Sun. November 8, 2009**	**Mon. December 28, 2009**	**January 16-20, 2010** Your Lab time In your Lab		Per the schedule from the registrar's office
Exams Times:	7:00 – 9:00 PM	7:00 – 9:00 PM			
Exams Places:	To be announced	To be announced			
Important Dates:	Last day to drop the course without a permanent record	Last day to drop the course with "W" grade	Last day to drop all courses with "WP/WF" Thru Registrar's office.		
	Wednesday October 14, 2009	**Wednesday November 11, 2009**	**Wednesday January 20, 2010**		

Note #1: Final Exam is **coordinated** and **comprehensive** (i.e. it is common for all sections and covers chapter 1-7 as described in the syllabus and class notes). Lab Final will be given by the Lab instructor in the Lab during the normal Lab session. **Major Exams are also coordinated**.

Note #2: According to the rules and regulations of KFUPM, attendance is **MANDATORY**. More than **8** unexcused absences will be reported to the registrar office and result in a **GRADE of DN** regardless of the student's grade.

Note #3: It is your responsibility to solve the ***practice problems*** as soon as the material is covered in the class. Solution will be posted on **WebCT**.This ***practice problems*** set will not be collected.

Note #4: Your instructor will give you other home work assignments which will be collected and graded. Quizzes will be given regularly based on the homework and the ***practice problems***..

Note #5: **A** design project will be assigned around week 11 and will be due at the end of week 13**.**

B. Tentative Course Outline and Schedule

Week	Date	Topics	Sections	Labs/Prob. Sessions
1	October 3-7	Binary Numbers, Number Base Conversions,	1.1-1.3	No Lab.
2	October 10-14	Octal & Hexadecimal Numbers, Complements, Signed Binary Numbers, Binary Codes	1.4-1.7	Introduction to Lab. Equipment, Exp#1: Binary & Decimal Numbers
3	October 17-21	Binary Logic, Boolean Algebra: Axioms, Theorems & Properties. Boolean functions, Digital Logic Gates	1.9, 2.1-2.4 2.7-2.8	No Lab.
4	October 24-28	Canonical & Standard Forms, More Logical Operations, Simplification of Boolean functions Using K-Maps, Product of Sums Simplification.	2.5-2.6 3.1-3.5	Exp#2: Digital Logic Gates
5	October 31- November 4	Don't-care Conditions, NAND, NOR, and Other Two Level Implementations, Exclusive-OR Function.	3.6-3.9	Exp#3: Introduction to LogicWorks **Exam # 1**
6	November 7-11	Combinational Logic: Analysis and Design Procedures, Code Conversion, Adder circuits.	4.1-4.4	Exp#4: Boolean Algebra
7	November 14-18	Subtractors, Decimal Adder, binary multiplier, Magnitude Comparator, Decoders.	4.5-4.8	Exp#5: Simplification
Eid Al-Adha Vacation November 19-December 4				
8	December 5-9	Encoders and Multiplexers, Random Access Memory.	4.9-4.11, 7.2, 7.3	Exp#6: Code Conversion
9	December 12-16	Programmable Logic, PLD'S, ROM, Programmable Logic Array, Programmable Array Logic.	7.5-7.7	Exp#7: Adders/Subtractors
10	December 19-23	Sequential Circuits, Latches, Flip-flops, Characteristic Tables	5.1-5.4	Exp#8: Multiplexers
11	December 26-30	Analysis of Clocked Sequential Circuits, State Reduction and Assignment.	5.4, 5.7	Exp#9: Design with ROM's **Exam # 2**
12	January 2-6	Flip-flop Excitation Tables, Design Procedure, Synthesis using different flip flops.	5.8	Exp#10: Flip-flops
13	January 9-13	Registers and Shift Registers	6.1, 6.2	Exp#11: Counters & Sequential Logic
14	January 16-20	Ripple Counters, Synchronous Counters and other counters.	6.3-6.5	**Lab Final**
15	January 23-27	Revision.		

C. Practice Problems

Chapter 1: 5,7,9,18,20,29,35
Chapter 2: 2,8, 12, 15,18,20
Chapter 3: 2,7,12,15,19,24
Chapter 4: 5,11,13,20,25,29,31,35
Chapter 7: 15,18,19,21,25
Chapter 5: 2,6,9,12,19
Chapter 6: 5,7,8,12,21