Topics of the CSE PhD Comprehensive Exam

Computer Networks:

Data Link Layer {chapter 3 of Tanenbaum's textbook}

- Data link layer design issues
- Error detection and correction
- Stop-and-Wait and Sliding window protocols and their analysis
- Example data link protocols

Medium Access Control {chapter 4 of Tanenbaum's textbook}

- The channel allocation problem
- Multiple access protocols
- Ethernet and Wireless LANs
- Data link layer switching, use of bridges, and VLANs

Network Layer {chapter 5 of Tanenbaum's textbook}

- Network layer design issues
- Routing algorithms
- Congestion control algorithms
- Quality of service
- Internetworking
- The Internet layer in the Internet

Transport Layer {chapter 6 of Tanenbaum's textbook}

- The transport service
- Elements of transport protocols
- Congestion Control
- The Internet transport protocol UDP
- The Internet transport protocol TCP

Application Layer {chapter 2 of Kurose's textbook / chapter 7 of Tanenbaum's textbook}

- Principles of Network Applications
- The Web and HTTP
- File Transfer: FTP
- Electronic Mail in the Internet
- DNS—The Internet's Directory Service
- Peer-to-Peer Applications

References:

1. Computer Networks by Andrew Tanenbaum and David Wetherall, Prentice Hall, 2014.
2. Computer Networking: A Top-Down Approach Featuring the Internet by Kurose and Ross, Addison Wesley, 2013.

Algorithms:

1. Divide and conquer.
    a. Alsuwaiyel: Chapter 6 + Chapter 2 Section 8.
    b. Cormen: Chapter 4 Section 5.
2. Dynamic programming.
    a. Alsuwaiyel: Chapter 7
3. Computational Geometry: Covex hull, Nearest neighbors, Voronoi diagrams.
    a. Alsuwaiyel: Chapter 18 Sections 1-4 + Chapter 19 Sections 1-3.
4. NP-complete problems.
    a. Alsuwaiyel: Chapter 10.
5. Network flow.
    a. Alsuwaiyel: Chapter 16 Sections 1-3.
6. Matching, Bipartite Matching.
    a. Alsuwaiyel: Chapter 17 Sections 1-3 and Section 6.
7. Approximation algorithms: Traveling Salesman Problem, Vertex Cover, Knapsack and Subset Sum problems.
    a. Alsuwaiyel: Chapter 15 Sections 1-4.
8. Randomized algorithms: Monte Carlo and Las Vegas Algorithms, Randomized Quicksort, The ball and Bin model, The birthday paradox.
    a. Alsuwaiyel: Chapter 14 Sections 1-3 + Section 7.
    b. Cormen: Chapter 5 Sections 1-2 + Section 4 (Only 4.1 and 4.2).

References:

1. Alsuwaiyel, M. H., Algorithms: Design Techniques and Analysis, World Scientific Publishers, 1999.
2. Cormen, T. H., Leiserson, C. E., Rivest, R. L. and Stein, C. Introduction to Algorithms, The MIT Press, Cambridge, 3rd edition, 2009.

Computer Architecture:

1. Instruction set architectures design.
   a. Basics of Computer Design. Performance Measures. Instruction Set Architecture (ISA) Characteristics and Classifications. CISC vs. RISC, The MIPS64 ISA. (Fourth Edition: Chapter 1, Appendix B)).
2. Instruction pipelining advanced ILP, software approaches to ILP, static/dynamic branch prediction, and performance.
   a. Exploiting Instruction-Level Parallelism (ILP): Basic Instruction Block, Loop Unrolling. Further Classification of Instruction Dependencies: Dependency Analysis and Graphs (Fourth Edition: Chapter 2.1, 2.2))
   b. Dynamic Hardware-Based Instruction Pipeline Scheduling: The Scoreboard, The Tomasulo Approach (Fourth Edition: Appendix A.7, Chapter 2.4, 2.5)
   c. Fundamental Dynamic Hardware-Based Branch Prediction Techniques: Branch-Target Buffer (BTB), Single-level, Correlating Two-Level, Gshare, and Hybrid Dynamic Branch Predictors. (Fourth Edition: Chapter 2.3, 2.9)
   d. Multiple Instruction Issue, CPI <1 Approaches: Superscalar, VLIW. Hardware-Based Speculation: Speculative Tomasulo. (Fourth Edition: Chapter 2.6-2.8)
   e. Data Parallelism & Loop-Level Parallelism (LLP) Analysis. GCD Test. Software Pipelining. FYI: Brief Introduction to Vector Processing. (Fourth Edition: Appendix G.1-3)
   f. Limits on ILP (chapter 3)
3. Hierarchical memory system, cache memory, virtual memory, performance and design tradeoffs
   a. Review of Memory Hierarchy & Cache Basics. 3Cs of Cache Misses, Cache Write Strategies & Performance. Multi-Level Cache. (Fourth Edition: Chapter 5.1 and Appendix C.1-C.3)
   b. The Memory Hierarchy: Main Memory Issues. Performance Metrics: Latency & Bandwidth. DRAM System Memory Generations. Basic Memory Bandwidth Improvement/Miss Penalty Reduction Techniques. (Fourth Edition: Chapter 5.3)
   c. Virtual Memory (Fourth Edition: Chapter 5.4 and 5.5)
4. Storage Systems
   a. Input/Output & System Performance Issues.(Fourth Edition: Chapter 6.1, 6.2, 6.4, 6.5)

   Parallel Architectures (Culler and Singh, Parallel Computer Architecture: A Hardware/Software Approach)
   b. Classification of Multiporcessors,
   c. Coherence Protocols for Shared and Distributed Memory systems (MSI, MESI, Dragon). Memory consistency protocols.
   d. Interconnection networks and performance.

References:

1. Hennessey & Patterson, Computer Architecture: A Quantitative Approach, Fifth edition.

Operating Systems:

1. Chapter 1: Introduction
2. Chapter 2: Systems Structures
3. Chapter 3: Process Concepts
4. Chapter 4: Multithreaded Programming
5. Chapter 5: Process Scheduling
6. Chapter 6: Synchronization
7. Chapter 7: Deadlock
8. Chapter 8: Memory Management Strategies
9. Chapter 9: Virtual Memory Management
10. Chapter 10: File Systems
11. Chapter 11: Implementing File Systems
12. Chapter 12: Mass Storage Management
13. Chapter 13: I/O Systems

References:

1. Operating Systems Concepts, 9th Edition Silbershaz, Galvin, Gagne, 2014