



King Fahd University of Petroleum and Minerals
Department of Electrical Engineering
EE 200 Digital Logic Circuit Design
Semester 052

Instructor: Dr. Wajih A. Abu-Al-Saud
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Office Hours: UT @ 11:00am – 12:00 pm
M @ 9:00 am – 12:00 pm, and by appointment.

Textbook: *Digital Design (3rd Edition)*, by M. M. Mano.

<u>Grade Distribution:</u>	<u>Points</u>
Major Exam I	15 %
Major Exam II	15 %
6 Quizzes	10 %
Homework	5 %
Design Project	5 %
Laboratory	20 %
Final Exam	30 %
Total	100 %

Regulations

1. University regulations regarding attendance are observed and enforced (a grade of DN will be given after the 5th unexcused absence). Only official excuses will be accepted and must be submitted no later than the second lecture after the excused absence.
2. Homework problems will be handed by the instructor at least a week before their due date. On the due date of each homework assignment, the solution will be posted on WebCT. Furthermore, another list of homework problems is given at the end for more practice. The solution of these problems will not be collected but you are highly encouraged to solve these problems too. You will get a quiz on the same material of the homework assignment in the lecture following the assignment due date.
3. Final exam will be comprehensive and common for all lecture sections.
4. On-line lectures will be available under WebCT which is maintained by the course coordinator (Dr. Mahmoud Dawoud). All students will have access to these lectures. All students are encouraged to access these lectures before attending the regular classes. A feed-back will be obtained from the students through questionnaires.
5. Selected weeks will be conducted fully on-line. You will study the material on-line. You will communicate with your instructor via WebCT communication tools. You will attend Wednesday classes of these weeks. In Wednesday class, you will have the chance to discuss the material and take a special quiz.

Wk	Day	Date	Topics	Text	Quiz & HW due	Laboratory/Tutorial
1	U T	12 Feb. 14 Feb.	Binary Numbers, Number Base Conversions	1.1-1.3		No Lab
2	U T	19 Feb. 21 Feb.	Octal & Hexadecimal Numbers, Complements, Signed Binary Numbers, Binary Codes	1.4-1.7		Intro. to Lab Equip. Exp#1: Binary & Decimal Numbers
3	U T	26 Feb. 28 Feb.	Binary Logic, Boolean Algebra: Axioms, theorems & Properties. Boolean functions, Digital Logic Gates	1.9, 2.1-2.4 2.7-2.8	HW 1 Due Quiz 1	No Lab.
4	U T	5 Mar. 7 Mar.	Canon. & Stand. Forms, More Logical Ops., Simp. of Bool. functions Using K-Maps, Prod. of Sums Simp.	2.5-2.6 3.1-3.4		Exp#2: Digital Logic Gates
5	U T	12 Mar. 14 Mar.	Don't-care Cond., NAND, NOR, and other 2-Level Imp., X-OR Function, Introduction to HDL.	3.5-3.8	HW 2 Due Quiz 2	Exp#3: Introduction to LogicWorks
6	U T	19 Mar. 21 Mar.	Subtractors, Decimal Adder, binary multiplier, Magnitude Comparator, Decoders.	3.9, 4.1-4.4		Exp#4: Boolean Algebra
Major Exam I, Wednesday, 22 March., 7:00 pm – 9:00 pm, OAB Building (Sections 1.1-3.8)						
7	U T	26 Mar. 28 Mar.	Subtractors, Decimal Adder, binary multiplier, Magnitude Comparator, Decoders.	4.5-4.8		Exp#5: Simplification
Midterm Break, Saturday and Sunday, 1-2 April						
8	T	4 Apr.	Encoders and Multiplexers, Random Access Memory.	4.9-4.10, 7.2, 7.3	HW 3 Due Quiz 3	Exp#6: Code Conversion
9	U T	9 Apr. 11 Apr.	Programmable Logic, PLD'S, ROM, Programmable Logic Array, Programmable Array Logic.	7.5-7.7		Exp#7: Adders/Subtractors
10	U T	16 Apr. 18 Apr.	Sequential Circuits, Latches, Flip-flops, Characteristic Tables	5.1-5.3	HW 4 Due Quiz 4	Exp#8: Multiplexers
11	U T	23 Apr. 25 Apr.	Analysis of Clocked Sequential Circuits, State Reduction and Assignment.	5.4, 5.6		Exp#9: Design with ROM's
Major Exam II, Saturday, 29 April, 7:00 pm – 9:00 pm, OAB Building (Sections 3.9-5.3)						
12	U T	30 Apr. 2 May	Flip-flop Excitation Tables, Design Procedure, Synthesis using different flip flops.	5.7		Exp#10: Flip-flops
13	U T	7 May 9 May	Registers and Shift Registers	6.1, 6.2	HW 5 Due Quiz 5	Exp#11: Counters & Sequential Logic
14	U T	14 May 16 May	Ripple Counters, Synchronous Counters and other counters.	6.3-6.5	HW 6 Due	Lab Final
15	U T	21 May 23 May	Review		Quiz 6	
16	U	21 May	Review			
Final Exam, To be scheduled by Registrar (Sections 1.1-6.5)						